In the Claims:

1. An integrated circuit arrangement ~~(140)~~, ~~having~~ comprising:

an electrically insulating insulating region, and ~~having~~

at least one sequence of regions which forms a capacitor ~~(144)~~ and which contains, in the order specified:

an electrode region ~~(34)~~ near the insulating region,

a dielectric region ~~(46)~~, and

an electrode region ~~(56)~~ remote from the insulating region,

the insulating region being part of an insulating layer ~~(14)~~ arranged in a plane,

the capacitor ~~(144)~~ and at least one active component ~~(142)~~ of the integrated circuit arrangement ~~(140)~~ being arranged on the same side of the insulating layer ~~(14)~~, ~~and~~

the electrode region ~~(34)~~ near the insulating region and ~~the~~ an active region ~~(84)~~ of the component ~~(142)~~ being arranged in a plane which lies parallel to the plane in which the insulating layer ~~(14)~~ is arranged, and

the capacitor and the active component forming a memory cell,

wherein at least one processor is contained in the integrated circuit arrangement.

2. The circuit arrangement ~~(140)~~ as claimed in claim 1, ~~characterized by~~further comprising at least one field-effect transistor ~~(142)~~, ~~whose~~ wherein at least one of:

a channel region ~~(84)~~ of the transistor is the active region, ~~the channel region (84) preferably being doped or undoped,~~

~~and/or whose~~a control electrode ~~(54)~~ of the transistor at least one of contains the same material ~~and/~~or material of the same dopant concentration as the electrode region ~~(56)~~ remote from the insulating region,

~~and/or whose~~ a control electrode insulating region ~~(42)~~ at least one of contains the same material ~~and/~~or a material having the same thickness as the dielectric region ~~(46)~~, ~~and/~~or

~~whose~~ the control electrode insulation region ~~(42)~~ at least one of contains a different material ~~and/~~or a material having a different thickness than the dielectric region ~~(46)~~.

3. The circuit arrangement ~~(140)~~ as claimed in claim 2, wherein at least one of:

the field-effect transistor ~~(122)~~ is a planar field-effect transistor,

~~and/or wherein~~ the transistor contains auxiliary terminal regions ~~(58, 59)~~, which have a doping with the same conduction type as ~~the~~ terminal regions ~~(80, 82)~~ of the transistor but with a dopant concentration that is smaller by at least one order of magnitude,

~~and/or wherein~~ the transistor contains auxiliary doping regions, which are arranged at least one of near the terminal regions ~~(80, 82) and/~~or near the auxiliary terminal regions ~~(58, 59)~~ and which have a doping with a different conduction type at least one of than the terminal regions ~~(80, 82) and/~~or than the auxiliary terminal regions ~~(58, 59)~~, ~~and/~~or

~~wherein~~ the control electrode ~~(54)~~ adjoins a region containing a metal-semiconductor compound~~, in particular a silicide region (92)~~.

4. The circuit arrangement ~~(140)~~ as claimed in claim ~~2 or~~ 3, wherein at least one of:

one terminal region ~~(80, 82)~~ of the transistor ~~(142)~~ or both terminal regions ~~(80, 82)~~ of the transistor ~~(142)~~ adjoin the insulating layer ~~(14)~~,

~~and/or wherein~~ at least one terminal region ~~(80, 82)~~ adjoins a region containing a metal-semiconductor compound, ~~preferably a silicide region (90, 96),~~

~~and/or wherein~~ a boundary area of at least one terminal region ~~(80, 82)~~ which is remote from the insulating region is further away from the insulating layer ~~(14)~~ than the active region ~~(84)~~, or

~~wherein~~ a boundary area of at least one terminal region ~~(80, 82)~~ which is remote from the insulating region is arranged nearer to the insulating layer ~~(14)~~ than a boundary area of the active region ~~(84)~~ which is remote from the insulating region.

5. The circuit arrangement ~~(140)~~ as claimed in ~~one of~~ claims 2 ~~to~~ 4, wherein at least one of:

spacers ~~(60, 62)~~ are arranged on both sides of the control electrode ~~(54)~~, ~~which spacers contain a different material than the control electrode (54), preferably silicon dioxide or silicon nitride, or which~~ and the spacers comprise a different material than the control electrode ~~(54)~~, ~~preferably silicon dioxide or silicon nitride,~~

~~and/or wherein~~ a spacer ~~(64, 66)~~ is arranged at at least one side of the electrode region ~~(56)~~ remote from the insulating region, ~~which spacer contains a different material than the electrode region (56) remote from the insulating region, preferably silicon dioxide or silicon nitride, or which~~and the spacer comprises a different material than the electrode region ~~(56)~~ remote from the insulating region, ~~preferably silicon dioxide or silicon nitride,~~ ~~and~~/or

~~wherein~~ a spacer ~~(62a)~~ arranged at the control electrode ~~(54)~~ and a spacer ~~(64a)~~ arranged at the electrode region ~~(56)~~ remote from the insulating region touch one another.

6. The circuit arrangement ~~(140)~~ as claimed in ~~one of~~ claims 2 ~~to~~ ~~5~~, wherein at least one of:

a terminal region ~~(82)~~ of the field-effect transistor ~~(142)~~ and the electrode region ~~(34)~~ of the capacitor ~~(144)~~ which is near the insulating region adjoin one another and have an electrically conductive connection at the boundary,

~~and/or wherein~~ the terminal region ~~(59a)~~ of the transistor ~~(152)~~ which adjoins the electrode region ~~(34)~~ near the insulating region does not adjoin a region containing a metal-semiconductor compound, ~~in particular does not adjoin a silicide region,~~ ~~and~~/or

wherein ~~the~~ another terminal region ~~(80a)~~ of the transistor adjoins a region ~~(70a)~~ containing a metal-semiconductor compound.

7. The circuit arrangement ~~(140)~~ as claimed in claim 6, wherein: ~~that~~

a side of the electrode region ~~(34)~~ near the insulating region which adjoins the terminal region ~~(82)~~ is longer than a side of the electrode

region ~~(34)~~ near the insulating region which lies transversely with respect to said side near the insulating region, ~~preferably being at least twice as long or at least five times as long, the transistor (142) preferably having a transistor width (W1) which is a multiple of the minimum feature size (F), preferably more than three-fold or more than five-fold,~~ or

wherein ~~a~~ the side of the electrode region ~~(34)~~ near the insulating region which lies transversely with respect to ~~that~~ the side of the electrode region ~~(34)~~ near the insulating region which adjoins the terminal region ~~(82)~~ is longer than the side adjoining the terminal region ~~(82)~~, ~~preferably at least twice as long or at least five times as long, the transistor (152) preferably having a transistor width (W2) which is less than three times the minimum feature size (F), preferably less than twice the minimum feature size (F)~~.

8. The circuit arrangement ~~(140)~~ as claimed in ~~one of the preceding claims~~claim 1, wherein at least one of:

the electrode region ~~(34)~~ near the insulating region is a monocrystalline region, ~~preferably a doped semiconductor region,~~

~~and/or wherein~~ at least one of the electrode region ~~(34)~~ near the insulating region ~~and/~~or the active region ~~(84)~~ has a thickness of less than 100 nanometers ~~or less than 50 nanometers~~,

~~and/or wherein~~ the active region ~~(84)~~ is a monocrystalline region, ~~preferably a semiconductor region which is doped or undoped,~~

~~and/or wherein~~ the insulating layer ~~(14)~~ adjoins, at one side, a carrier substrate ~~(12)~~, ~~preferably a carrier substrate which contains a semiconductor material or comprises a semiconductor material in particular silicon or monocrystalline silicon,~~

~~and/or wherein~~ the insulating layer ~~(14)~~ adjoins the electrode region ~~(34)~~ near the insulating region at ~~the other~~ a side other than the side at which the insulating layer adjoins the carrier substrate,

~~and/or wherein~~ the boundary areas ~~preferably~~ lie completely in two mutually parallel planes,

~~and/or wherein~~ the insulating layer ~~(14) contains an electrically insulating material, preferably an oxide, in particular silicon~~

~~dioxide, or~~ comprises an electrically insulating material, ~~preferably an oxide, in particular silicon dioxide,~~ ~~and/~~or

~~wherein~~ the active component ~~(142)~~ is a transistor~~, preferably a field-effect transistor, in particular a planar field-effect transistor~~.

9. The circuit arrangement ~~(140)~~ as claimed in ~~one of the preceding claims~~claim 1, wherein at least one of:

the dielectric region ~~(46) contains silicon dioxide or~~ comprises silicon dioxide,

~~and/or wherein~~ the dielectric region ~~(46)~~ comprises a material having a dielectric constant of greater than 4 ~~or greater than 10 or greater than 50~~,

~~and/or wherein~~ the electrode region ~~(56)~~ remote from the insulating region ~~contains silicon, preferably polycrystalline silicon, or~~ comprises silicon, ~~preferably polycrystalline silicon,~~

~~and/or wherein~~ the electrode region ~~(56)~~ remote from the insulating region ~~contains a metal or~~ comprises a metal,

~~and/or wherein~~ the electrode region ~~(56)~~ remote from the insulating region contains a low-impedance material, ~~preferably titanium nitride, tantalum nitride, rubidium or highly doped silicon-germanium,~~ ~~and/~~or

~~wherein~~ the electrode region ~~(56)~~ remote from the insulating region adjoins a region containing metal-semiconductor compounds~~, in particular a silicide region (96)~~.

10. The circuit arrangement ~~(140)~~ as claimed in ~~one of the preceding claims~~claim 1, wherein at least one of:

the ~~circuit arrangement contains at least one~~ processor, ~~preferably~~is a microprocessor,

~~and/or wherein~~ the capacitor ~~(154)~~ and the active component ~~(152)~~ form a memory cell ~~(150)~~, ~~in particular in a dynamic RAM memory unit,~~ ~~and/~~or

~~wherein~~ a memory cell contains either a capacitor ~~(152)~~ and only one transistor ~~(152)~~ or a capacitor ~~(Cs)~~ and more than one transistor ~~(M1 to M3), preferably three transistors (M1 to M3)~~.

11. A method for fabricating an integrated circuit arrangement ~~(140)~~ with a capacitor ~~(144)~~, a transistor, and a processor, ~~in particular a circuit arrangement (140) as claimed in one of the preceding claims,~~ in which the following method steps are performed without any restriction by the order specified:

~~provision of~~ providing a substrate ~~(10)~~ containing an insulating layer ~~(14)~~ made of electrically insulating material and a semiconductor layer ~~(16)~~, the insulating layer being planar and having an electrically insulating insulating region,

patterning ~~of~~ the semiconductor layer ~~(16)~~ in order to form at least one electrode region ~~(34)~~ near the insulating region for ~~a~~ the capacitor and in order to form at least one active region ~~(84)~~ for ~~a~~ the transistor ~~(142)~~,

after the patterning of the semiconductor layer, ~~(16)~~ ~~production of~~ producing at least one dielectric layer ~~(42, 46)~~,

after the production of the dielectric layer ~~(42, 46)~~, producing ~~production of~~ an electrode layer ~~(41)~~, and

~~formation of~~ forming an electrode ~~(56)~~ of the capacitor ~~(144)~~ which is remote from the insulating region in the electrode layer ~~(41)~~,

wherein the capacitor and the transistor are arranged on the same side of the insulating layer,

the electrode region near the insulating region and the active region of the transistor are arranged in a plane which lies parallel to the plane in which the insulating layer is arranged, and

the capacitor and the transistor form a memory cell.

12. The method as claimed in claim 11, ~~characterized by~~ further comprising at least one of the following steps:

~~application of~~ applying at least one auxiliary layer ~~(18, 20)~~ to the semiconductor layer ~~(16)~~ prior to patterning, ~~preferably a silicon nitride layer (20) and/or an oxide layer (18), the auxiliary layer (20) preferably serving as a hard mask during the patterning of the semiconductor layer (16),~~

~~and/or~~ doping ~~of~~ a channel region ~~(84)~~ of the transistor ~~(142)~~, ~~preferably before the production of the dielectric layer (42, 46),~~

carrying out of a thermal oxidation in order to form a rounding oxide ~~(26, 28)~~, ~~preferably before the formation of the electrode layer (41),~~

~~and/or~~ doping ~~of~~ the electrode ~~(34)~~ near the insulating region, ~~preferably before the production of the dielectric layer (42, 44, 46),~~

~~and/or production of~~ producing the dielectric layer ~~(42, 46)~~ at the same time as a dielectric layer at the active region ~~(84)~~ of the transistor ~~(122)~~, or

~~and/or formation of~~ forming a control electrode ~~(54)~~ of the transistor ~~(142)~~ at the same time as the formation of the electrode region ~~(56)~~ remote from the insulating region.

13. The method as claimed in claim 11 ~~or 12~~, ~~characterized by~~ further comprising at least one of the following steps:

~~formation of~~ forming auxiliary terminal regions ~~(58, 59)~~ with a lower dopant concentration than terminal regions ~~(80, 82)~~ of the transistor ~~(142)~~, ~~preferably after the patterning of a control electrode (54) of the transistor (142),~~

~~and/or formation of~~forming auxiliary doping regions, ~~preferably before the patterning of the control electrode (54),~~

~~application of~~applying a further auxiliary layer ~~(60 to 66)~~ after the patterning of a control electrode ~~(54)~~ of the transistor ~~(142)~~, ~~preferably a silicon nitride layer or a silicon dioxide layer, in particular a TEOS layer,~~or

~~and/or~~ anisotropically etching ~~of~~ the further auxiliary layer ~~(60 to 66)~~.

14. The method as claimed in ~~one of~~ claims 11 ~~to 13~~, ~~characterized by~~further comprising at least one of the following steps:

carrying out of a selective epitaxy on uncovered regions made of semiconductor material ~~(16)~~ at least one of after the formation of the electrode region ~~(56)~~ remote from the insulating region ~~and~~/or after the patterning of a control electrode ~~(54)~~ of the transistor ~~(142)~~, or

~~and/or~~ doping ~~of~~ terminal regions ~~(70, 72)~~ of the transistor ~~(122)~~ at least one of after the formation of the electrode region ~~(56)~~ remote from the insulating region ~~and~~/or after the patterning of the control electrode ~~(54) and preferably after the epitaxy~~.

15. The method as claimed in ~~one of~~ claims 11 ~~to 14~~, further comprising ~~characterized by~~ the following step: ~~and/or selective formation of~~ selectively forming a metal-semiconductor compound~~, in particular selective silicide formation,~~ at least one of on the electrode layer ~~(54)~~ ~~and/~~or on uncovered semiconductor regions ~~(16)~~.